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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,162	01/11/2002	Shahram Mostafazadeh	NSC1P225R	3102

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EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,162	MOSTAFAZADEH ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2 and 4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Transitional After Final Practice

1. The Pre-Brief Appeal Conference decides to reopen prosecution. The rejection in previous office action has been withdrawn and a new ground(s) of rejection is made.

Reissue Applications

2. Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. 6,117,710 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Affidavit

3. The affidavit filed on 05/02/2005 under 37 CFR 1.131 had been re-considered but is ineffective to overcome the Melton et al. reference.

4. The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the Melton et al. reference to either a constructive reduction to practice or an actual reduction to practice. Specifically, the affidavit establishes conception prior to March 26, 1996. However, the affidavit fails to provide

evidence that diligence exists from the date of conception to the date of constructive reduction to practice, the effective date of the instant reissue application. Accordingly, the affidavit is inadequate to disqualify the Melton et al. US patent No. 5,844,315 as prior art against the applicant.

5. The above statement had been stated in the Office action mailed 09/07/2005. Applicant failed to provide evidence that diligence exists in Response D received on 10/10/2005. Accordingly, it is adequate to use the Melton et al. US patent No. 5,844,315 as prior art against the instant invention.

Claim Objections

6. Claim 2 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Limitations of claim 2 are already recited in the step of electrically connecting of claim 1.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1-2 and 4-5 are rejected under 35 U.S.C. 102(a) as being anticipated by Melton et al. US 5,844,315.

Re claim 1, the Melton et al. reference discloses a method comprises:

forming a flat lead frame 22 including a plurality of leads 13 *extending radially from a central opening 39 (fig. 1)*, the lead frame having opposing upper and lower surfaces 19 and 17 (*"lead frame 22 comprises an outer ring element 35 and a plurality of metallic leads 16 that extend inwardly from outer ring element 35, each metallic lead 16 having a die proximate end 13. Die proximate ends 13 define an opening that is sized and shaped to receive integrated circuit die 12"*, col. 2, lines 47-52);

mounting the lead frame 22 and an integrated circuit die 12 onto a strip of adhesive tape 38 *("molding support 38 is formed of a flexible polyimide tape having an adhesive coating for temporarily securing integrated circuit die 12 and lead frame 22 during processing", col. 2, lines 55-59)* such that a lower surface 32 of the die 12 contacts the adhesive tape 38 and the die 12 is located in a central opening 39, and the lower surface 17 of the lead frame 22 also contacts the adhesive tape 38 *(fig. 2)*;

electrically connecting bond pads 36 on a top surface 28 of the die 12 to associated lead frame leads 13 using wire bonding 18 with the adhesive tape 38 in place such that the adhesive tape 38 holds the die 12 and lead frame 22 in place during the wire bonding operation *(fig. 4)*;

forming a plastic casing 21 over an upper surface 28 of the die 12 and the upper surface 19 of the lead frame 22 wherein the plastic casing 21 comes into contact with the adhesive tape 38 such that a lower surface 24 of the plastic casing 21 is substantially co-planar with the lower surface 17 of the lead frame 22 and the lower surface 32 of the die 12 *(using a dispensing approach* over an upper surface of the die

and the upper surface of the lead frame, *the dispensed polymeric precursor is an epoxy resin, "is applied to active face 28 of integrated circuit die 12, inner face 24 of metallic leads 16, wire leads 18, ... as well as exposed regions of molding support 38", col. 3, lines 54-57, the "resulting polymeric body 14 encapsulates active face 28 of the integrated circuit die 12, the plurality of wire leads 18, inner surface 19 ... thereby protecting them from environmental exposure and damage experienced during normal use of microelectronic package 10", col. 4, lines 15-20, and fig. 6)*; and

removing the adhesive tape 38 after forming the plastic casing 21 to expose the lower surface 32 of the die 12 and the lower surface17 of the lead frame 22 whereby exposed portions of the lead frame17 form the only externally accessible I/O contacts for the package 10 and plastic material fills at least portions of gaps between adjacent leads, such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing 21, the lead frame 22 and the die 12 *("ensure that metallic leads 16 are electrically discrete", "first surface 24, non-active face 32 and outer surface 17 cooperate to form planar surface 37"*, col. 4, lines 8, 22-26 and 66-67).

Re claim 2, the die includes a plurality of die bond pads 36, and the method further comprises the step of electrically connecting each of the die bond pads to a selected one of the plurality of leads 13, the step of electrically connecting comprises wire bonding, col. 2, line 60 to col. 3, line 8.

Re claims 4-5, the forming the lead frame step comprises etching or stamping a metal sheet, col. 2, lines 43-45.

Claim Rejections - 35 USC § 103

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claims 1-2 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Djennas et al. US 5,474,958.

The Djennas et al. reference discloses methods for making semiconductor device having no die supporting surface.

In the *first embodiment*, figs. 4-6, the Djennas et al. reference discloses a method for making semiconductor device having no die supporting surface comprising: forming a flat lead frame including a plurality of leads extending radially from a central opening, "no tie bars, such as shown in FIG. 1 of the prior art", col. 4, lines 10-11, the lead frame having opposing upper and lower surface; the lead frame and an integrated circuit die are mounted onto a supporting work holder; molding a plastic casing over an upper surface of the die and the upper surface of the lead frame; the die includes a plurality of die bond pads so that "the active surface of the semiconductor die 22 is wire bonded to the plurality of conductors 12", col. 4, lines 20-22.

In the *third embodiment* of figs. 9-10, "the inactive surface of the wire bonded semiconductor die 22 is placed directly on a lower mold platen 92 includes a vacuum line 94 ... aids in the prevention of flash ... a heat sink (not illustrated) can be attached to the exposed inactive surface of the die 22 for enhanced thermal dissipation. In addition to the aforementioned advantages of device 58, another advantage to device 90 is that the total thickness of the device has been decreased because the package

body 96 is not a total encapsulation of the semiconductor die 22... a heat sink (not illustrated) can be attached to the exposed inactive surface of the die 22 for enhanced thermal dissipation ... It should be obvious that although device 90 is illustrated ..., other external leads configurations are possible", col. 6, lines 19-50.

The two embodiments do not use removable tape to provide a temporary die supporting surface but use the mold platen or supporting work holder.

However, in the *sixth embodiment*, figs. 18-20, a "removable tape 148 is affixed to the bottom surface of the substrate 100 including the die cavity 102 ... the tape 148 provides a temporary die supporting surface whereupon the semiconductor die 22 is placed", col. 9, lines 6-12; the step of forming the plastic casing comprises molding plastic onto the upper surfaces of the die and the substrate, fig. 19; "the removal of the tape 148 from the bottom of the substrate 100 after the step of molding", col. 9, lines 49-51, whereby exposed portions of the substrate form the only externally accessible I/O contacts for the package, fig. 20.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the first and third embodiment formation of Djennas et al. *the adhesive tape peeling technique of the sixth embodiment of Djennas et al.* because *the adhesive tape technique* would provide the first and third embodiment formation with "a temporary die supporting surface whereupon the semiconductor die is placed" without the need of vacuum.

Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the sixth embodiment with the lead frame of the first

and/or third embodiment because the lead frame of the first and/or third embodiment would provide the sixth embodiment with "plurality of conductors extending toward the periphery of the semiconductor die" from the lead frame with more flexibility of connection.

With this combination, the exposed portions of the leads form the only externally accessible I/O contacts for a resulting integrated circuit package, these only externally accessible I/O contacts at the lower surfaces of the leads would be used to solder the package to the circuit board to electrically connect the package to the circuit board. Further, the Djennas reference teaches "the external portion of the leads can be in any surface mount or through hole configuration... a heat sink may be attached to the inactive surface of the semiconductor die in any of the embodiments provided that the inactive surface is at least partially exposed" (col. 12).

11. Claims 1-2 and 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melton et al. US 5,844,315 in combination with Djennas et al. US 5,474,958 and Ogawa et al. US 5,252,855.

The Melton et al. reference discloses a method substantially the same as the instant invention but lacks using molding technique for forming a plastic casing as stated in the above.

The Djennas et al. reference discloses substantially all of the instant invention and ignores how the conventional lead frame is formed.

The Ogawa et al. reference discloses a method of packaging an integrated circuit, fig. 5, comprising:

providing a lead frame including a plurality of leads 1 and a central opening, the lead frame is made by punching or by etching a plate composed of a copper alloy or an iron alloy, col. 1, lines 13-16, having opposing upper and lower surfaces;

mounting the lead frame 1 and an integrated circuit die 4 onto a strip of adhesive tape 2 as element mounting member such that a lower surface of the die contacts the adhesive tape and the die is located in the central opening and the lower surface of the lead frame also contacts the adhesive tape such that the lower surface of the die and the lower surface of the lead frame are substantially co-planar;

electrically connecting bond pads on a top surface of the die to associated lead frame leads with thin metal wire 5, fig. 5.

The Ogawa et al. reference does not teach

forming a plastic casing over an upper surface of the die and the upper surface of the lead frame wherein the molded plastic casing comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die; and

removing the adhesive tape after molding the plastic casing to expose the lower surfaces of the die and the leads, whereby exposed portions of the leads form the only external accessible I/O contacts for a resulting integrated circuit package and plastic material fills at least portions of gaps formed between adjacent leads such that the

lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the known semiconductor package formation of Ogawa et al. with the steps of casing formation and the adhesive tape removing of Melton et al. because the steps of casing and tape removing of Melton et al. would be selected in the manufacturing process to complete the package device as disclosed by Ogawa et al. and to protect the active face, the wire leads and inner surface of the die as taught by Melton et al. This combination will ensure the adhesive tape holds the die and lead frame in place during the wire bonding operation, the molded plastic casing comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die, and to expose the lower surfaces of the die and the leads, whereby exposed portions of the leads form the only external accessible I/O contacts for a resulting integrated circuit package and plastic material fills at least portions of gaps formed between adjacent leads such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die.

The combination does not disclose the plastic casing being formed by molding.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the Ogawa/Melton combination with the molding step

of the Djennas et al. reference as the molding step of Djennas et al. would be selected in accordance with the packaging process as taught by the combination. The choice of different lead frames, with radial or non-radial leads both without the die supporting surface, has no impact on the type of lead frame in the assembly of the package in terms of the thickness of the finished device as mentioned by both Melton and Ogawa et al. references. The molding technique of Djennas et al. would help in "the prevention of flash which may occur as a result of transferring the resin encapsulant into the mold cavity under high pressure" col. 6, lines 28-31.

Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the first and third embodiments formation of Djennas et al. with the lead frame *and the prior-art adhesive tape* of Ogawa et al. because the lead frame and adhesive tape of Ogawa would provide the package formation of Djennas et al. with an appropriate lead frame and an element-mounting member (*Ogawa et al.'s* col. 1, line 32 and col. 2, line 10).

With this combination, the exposed portions of the leads form the only externally accessible I/O contacts for a resulting integrated circuit package, these only externally accessible I/O contacts at the lower surfaces of the leads would be used to solder the package to the circuit board to electrically connect the package to the circuit board. Further, the Djennas reference teaches "the external portion of the leads can be in any surface mount or through hole configuration... a heat sink may be attached to the inactive surface of the semiconductor die in any of the embodiments provided that the inactive surface is at least partially exposed" (col. 12).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP

05/12/2006

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